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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **NAKATA, Shunji et al.** Group Art Unit: **2816**

Serial No.: **09/871,810** Examiner: **Cassandra F. COX**

Filed: **June 4, 2001** P.T.O. Confirmation No.: 1974

For: **ADIABATIC CHARGING REGISTER CIRCUIT**

INFORMATION DISCLOSURE STATEMENT PURSUANT TO 37 CFR 1.97(b)

Commissioner for Patents
Washington, D.C. 20231

May 1, 2003

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. One copy of each of these documents is attached.

No fee or certification is required in connection with this Information Disclosure Statement, since it is being submitted prior to the issuance of a first official action on the merits following the **Request for Continued Examination** (RCE) in the above-identified patent application.

JP 8-335873 claims conventional priority based on U.S. Patent No. 5,521,538.

JP 8-335873 describes a logic circuit with low power consumption by using an adiabatic charging logic. It concerns decreasing power consumption in a combination logic circuit, but not in a clock signal in a register circuit. Further, it does not teach the inequality in claim 1 of the present invention.

William C. Athas, "Energy-Recovery CMOS", Low Power Design Methodologies, J. M. Rabaey and M. Pedram (Kluwer Academic Publishers, 1996) Chap. 4, pages 65-72.

On page 71 of **Athas**, equation 4.10 shows that the power consumption is $E=(RC/T)CV^2$, where RC is a time constant of a circuit and T is time duration required for charging level of a pulse.

A circuit proposed by this article is called an adiabatic logic or a charge recycle logic. When time duration T is sufficiently larger than RC, the power consumption becomes close to zero.

However, the circuit differs from a CMOS circuit, it has been considered that the application of the circuit to a register circuit is impossible.

William C. Athas, et al., "A Low-Power Microprocessor Based on Resonant Energy", IEEE Journal of Solid-State Circuits, vol. 32, No. 11, November 1997, pages 1963-1701.

Fig. 5 of **Athas et al.** shows an energy-recovery latch (E-R latch) circuit in which the power consumption of a clock signal is decreased by recycling energy of a clock signal.

However, this circuit differs from our circuit, and moreover it has the disadvantage of short-circuit current which flows from power source to ground directly (see page 4, line 19 of the specification of the instant application).

The above information is presented so that the Patent and Trademark Office can determine any materiality thereof to the claimed invention. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

The Commissioner is authorized to charge our Deposit Account No. 01-2340 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

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Enclosures: PTO-1449 and references (5)